POINTER PROCESSING AND PATH BIP-8 COMPUTATION FOR LARGE CONCATENATED PAYLOADS

CROSS REFERENCE TO RELATED APPLICATIONS

now U.S. Patent # 6,938,395

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MICROFICHE APPENDIX

Not applicable.

TECHNICAL FIELD

The present invention relates to optical communication networks, and in particular to performing pointer processing and path BIP-8 computation for large concatenated payloads within processing nodes of such a network.

BACKGROUND OF THE INVENTION

Processing network nodes in current optical networks employing CMOS technology are limited by the speeds of this technology, which are well below currently available speeds of transmitting data over fibre optic links in such networks. In addition, at a network processing node, data may come from several different sources, on different connections and at different line clocks. However, at the node, all data must be processed at a local system clock. Accordingly, pointer processor systems are used within processing network nodes to perform timing adjustments on incoming data, by converting the incoming data from a line clock domain to a local system clock domain or 'shelf-time' domain.

In order to be able to handle large data frames, pointer processors usually comprise several integrated circuits. In turn, each integrated circuit may comprise a plurality of processing strips, with each processing strip having a limited data processing capacity. A known pointer processor design for SONET (Synchronous Optical Network) or SDH (Synchronous Digital